

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 63-191240

(43)Date of publication of application : 08.08.1988

(51)Int.Cl.

G06F 11/16

G06F 15/16

G06F 15/16

(21)Application number : 62-024306

(71)Applicant : NISSIN ELECTRIC CO LTD

(22)Date of filing : 03.02.1987

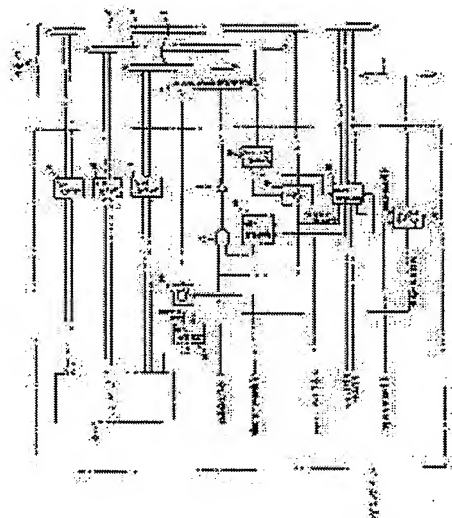
(72)Inventor : NAKANISHI KAZUO

(54) MULTI-PROCESSOR SYSTEM

(57)Abstract:

PURPOSE: To prevent the total discontinuation of a multi-processor system by separating logically only a processor having a fault from the system

CONSTITUTION: When a processor P has a fault among plural processors, a fault occurrence signal is delivered to a system state monitor signal line from the processor P. An optional processor monitoring the state of said signal line decides the occurrence of the fault with detection of the fault occurrence signal. A processor detecting means calls successively other processors to detect and specify a faulty one and gives the control commands to the faulty processor for stopping, resetting, interruption inhibiting actions, etc., based on the address signal of an address bus (a) and the data of a data bus (d). Thus the faulty processor stops the operation of a CPU, etc., resets each part and inhibits the interruptions supplied from an input/output control part, etc., based on the given control commands. Then the faulty processor is separated logically from a multi-processor system.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's
decision of rejection]

[Date of extinction of right]